

Appl. No. 10/711,916
Amtd. dated August 17, 2006
Reply to Office action of June 26, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A boost circuit capable of boosting a reference voltage into an
5 output voltage, the boost circuit comprising:

a main transistor electrically connected to the output voltage;

an auxiliary transistor electrically connected to the output voltage;

a pre-charge circuit electrically connected to the main transistor and the auxiliary
transistor for pre-charging the main transistor and the auxiliary transistor, the
10 pre-charge circuit comprising:

a first PMOS transistor;

a second PMOS transistor electrically connected between the first PMOS
transistor and the main and the auxiliary transistors; and

a level shift circuit electrically connected to the second PMOS transistor and
the output voltage for transferring the output voltage to the second PMOS
transistor according to a switch voltage; and

15 a voltage detector electrically connected to the auxiliary transistor and the reference
voltage for controlling the auxiliary transistor according to the reference
voltage.

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2 (original): The boost circuit of claim 1, wherein the main transistor is a triple-welled
NMOS.

25 3 (original): The boost circuit of claim 1, wherein the auxiliary transistor is a triple-welled
NMOS.

4 (original): The boost circuit of claim 1, wherein the voltage detector disables the

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auxiliary transistor when detecting that the reference voltage is higher than a predetermined voltage.

5 (cancelled).

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6 (original): The boost circuit of claim 1 further comprising a re-charge module electrically connected to the main transistor for re-charging the main transistor.

7 (original): The boost circuit of claim 6, wherein the re-charge module comprises:

10 a stable transistor;
a main re-charge transistor electrically connected between the stable transistor and the main transistor for re-charging the main transistor according to a voltage level of the stable transistor; and
a stable re-charge transistor electrically connected between the stable transistor and
15 the main transistor for re-charging the stable transistor according to a voltage level of the main transistor.

8 (currently amended): A boost circuit capable of boosting a reference voltage into an output voltage, the boost circuit comprising:

20 a main transistor electrically connected to the output voltage;
a pre-charge circuit electrically connected to the main transistor for pre-charging the main transistor;
a stable transistor;
a main re-charge transistor electrically connected between the stable transistor and
25 the main transistor for re-charging the main transistor according to a voltage level of the stable transistor; [[and]]
a stable re-charge transistor electrically connected between the stable transistor and the main transistor for re-charging the stable transistor according to a voltage

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level of the main transistor;
an auxiliary transistor electrically connected to the output voltage; and
a voltage detector electrically connected to the reference voltage and the auxiliary
transistor for controlling the auxiliary transistor according to the reference
5 voltage.

9 (cancelled).

10 (currently amended): The boost circuit of ~~claim 9~~ claim 8, wherein the voltage detector
10 disables the auxiliary transistor when detecting that the reference voltage is higher
than a predetermined voltage.

11 (new): A boost circuit capable of boosting a reference voltage into an output voltage,
the boost circuit comprising:
15 a main transistor electrically connected to the output voltage;
a re-charge module electrically connected to the main transistor for re-charging the
main transistor, the re-charge module comprising:
a stable transistor;
a main re-charge transistor electrically connected between the stable transistor
20 and the main transistor for re-charging the main transistor according to a
voltage level of the stable transistor; and
a stable re-charge transistor electrically connected between the stable transistor
and the main transistor for re-charging the stable transistor according to a
voltage level of the main transistor;
25 an auxiliary transistor electrically connected to the output voltage;
a pre-charge circuit electrically connected to the main transistor and the auxiliary
transistor for pre-charging the main transistor and the auxiliary transistor; and
a voltage detector electrically connected to the auxiliary transistor and the reference

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voltage for controlling the auxiliary transistor according to the reference voltage.

12 (new): The boost circuit of claim 11, wherein the main transistor is a triple-welled
5 NMOS.

13 (new): The boost circuit of claim 11, wherein the auxiliary transistor is a triple-welled
NMOS.

10 14 (new): The boost circuit of claim 11, wherein the voltage detector disables the
auxiliary transistor when detecting that the reference voltage is higher than a
predetermined voltage.